

DATA SHEET

TDA1517; TDA1517P 2 x 6 W stereo power amplifier

Product specification
Supersedes data of 2002 Jan 17

2004 Feb 18



2 x 6 W stereo power amplifier**TDA1517; TDA1517P****FEATURES**

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/standby switch
- AC and DC short-circuit safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs ($V_P = 0\text{ V}$)
- No switch-on/switch-off plop
- Electrostatic discharge protection.

GENERAL DESCRIPTION

The TDA1517 is an integrated class-B dual output amplifier in a plastic single in-line medium power package with fin (SIL9MPF), a plastic rectangular-bent single in-line medium power package with fin (RBS9MPF) or a plastic heat-dissipating dual in-line package (HDIP18). The device is primarily developed for multi-media applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		6.0	14.4	18.0	V
I_{ORM}	repetitive peak output current		–	–	2.5	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
I_{sb}	standby current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$ Z_i $	input impedance		50	–	–	$\text{k}\Omega$
P_o	output power	$R_L = 4\ \Omega$; THD = 0.5%	–	5	–	W
		$R_L = 4\ \Omega$; THD = 10%	–	6	–	W
SVRR	supply voltage ripple rejection	$f_i = 100\text{ Hz to }10\text{ kHz}$	48	–	–	dB
α_{CS}	channel separation		40	–	–	dB
G_v	closed loop voltage gain		19	20	21	dB
$V_{no(rms)}$	noise output voltage (RMS value)		–	50	–	μV
T_c	crystal temperature		–	–	150	$^{\circ}\text{C}$

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1517/N3	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1
TDA1517/N3/S5	RBS9MPF	plastic rectangular-bent single in-line medium power package with fin; 9 leads	SOT352-1
TDA1517P	HDIP18	plastic heat-dissipating dual in-line package; 18 leads	SOT398-1

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BLOCK DIAGRAM

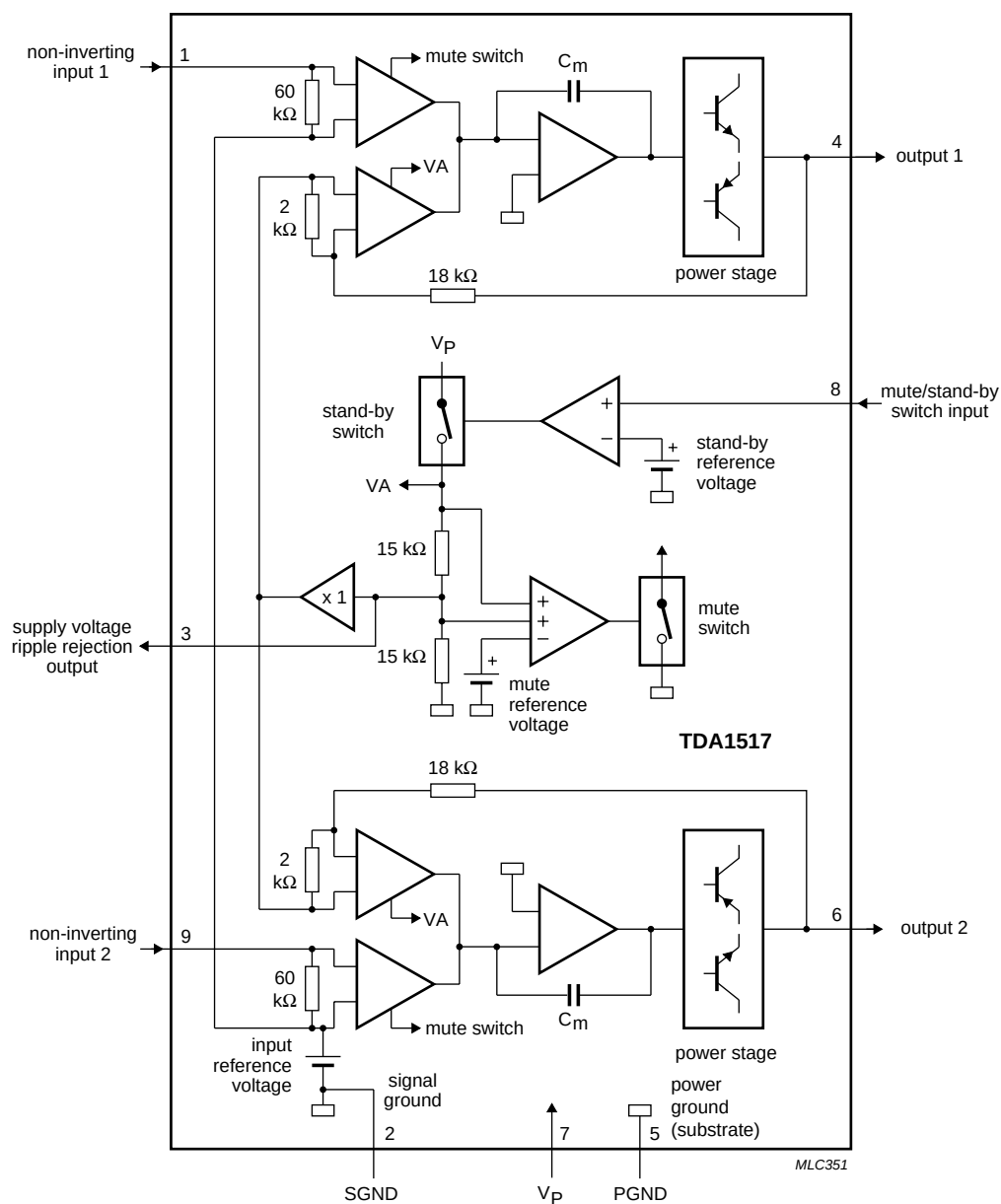


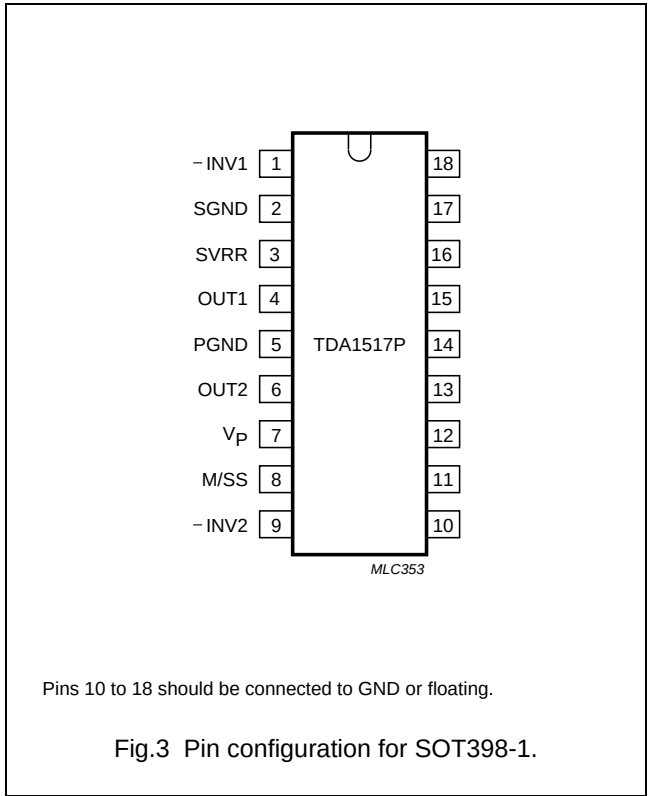
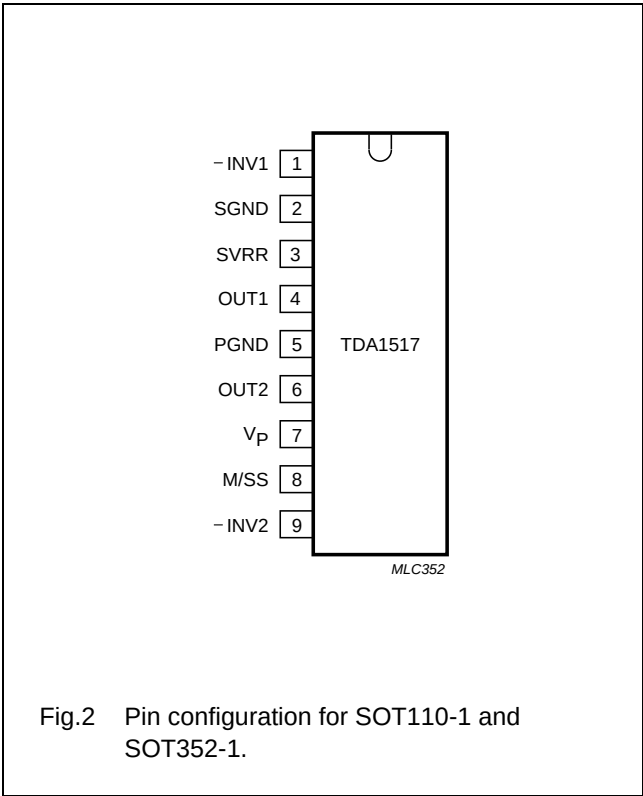
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
SGND	2	signal ground
SVRR	3	supply voltage ripple rejection output
OUT1	4	output 1
PGND	5	power ground
OUT2	6	output 2
V _P	7	supply voltage
M/SS	8	mute/standby switch input
–INV2	9	non-inverting input 2



FUNCTIONAL DESCRIPTION

The TDA1517 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 20 dB. A special feature of the device is the mute/standby switch which has the following features:

- Low standby current (<100 μA)
- Low mute/standby switching current (low cost supply switch)
- Mute condition.

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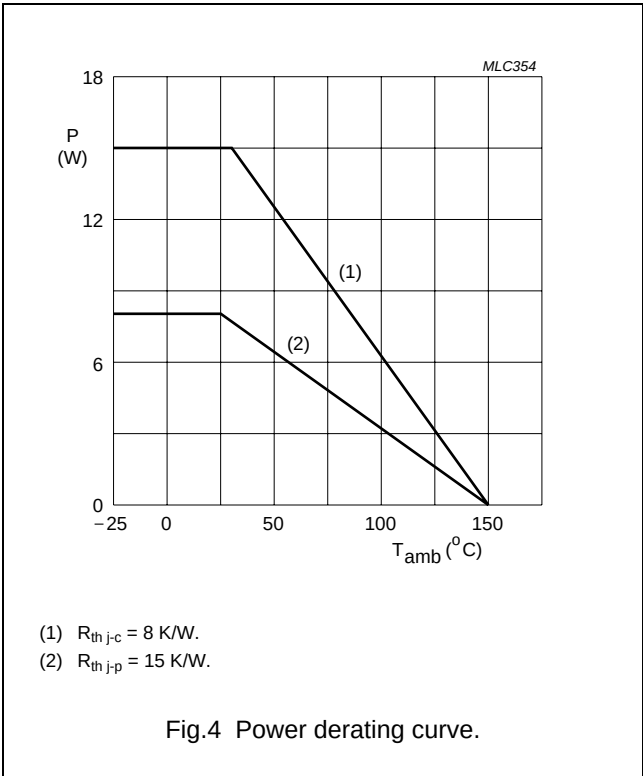
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage	operating	–	18	V
		no signal	–	20	V
V _{P(sc)}	AC and DC short-circuit safe voltage		–	18	V
V _{P(r)}	reverse polarity		–	6	V
ERG _O	energy handling capability at outputs	V _P = 0 V	–	200	mJ
I _{OSM}	non-repetitive peak output current		–	4	A
I _{ORM}	repetitive peak output current		–	2.5	A
P _{tot}	total power dissipation	see Fig.4	–	15	W
T _{stg}	storage temperature		–55	+150	°C
T _{amb}	operating ambient temperature		–40	+85	°C
T _c	crystal temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	TYPE NUMBER	PARAMETER	VALUE	UNIT
R _{th(j-c)}	TDA1517/N3; TDA1517/N3/S5	thermal resistance from junction to case	8	K/W
R _{th(j-p)}	TDA1517P	thermal resistance from junction to pins	15	K/W
R _{th(j-a)}	TDA1517/N3; TDA1517/N3/S5; TDA1517P	thermal resistance from junction to ambient	50	K/W



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DC CHARACTERISTICS

$V_P = 14.4\text{ V}$; $T_{\text{amb}} = 25\text{ °C}$; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
$I_{q(\text{tot})}$	total quiescent current		–	40	80	mA
V_O	DC output voltage		–	6.95	–	V
Mute/standby switch						
V_8	switch-on voltage level	see Fig.5	8.5	–	–	V
Mute condition						
V_O	output signal in mute position	$V_{l(\text{max})} = 1\text{ V}$; $f_i = 20\text{ Hz to }15\text{ kHz}$	–	–	2	mV
Standby condition						
I_{sb}	DC current in standby condition		–	–	100	μA
V_{sw}	switch-on current		–	12	40	μA

Note

1. The circuit is DC adjusted at $V_P = 6\text{ to }18\text{ V}$ and AC operating at $V_P = 8.5\text{ to }18\text{ V}$.

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AC CHARACTERISTICS

$V_P = 14.4\text{ V}$; $R_L = 4\ \Omega$; $f = 1\text{ kHz}$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%; note 1	4	5	–	W
		THD = 10%; note 1	5.5	6.0	–	W
THD	total harmonic distortion	$P_o = 1\text{ W}$	–	0.1	–	%
f_{lr}	low frequency roll-off	at –3 dB; note 2	–	45	–	Hz
f_{hr}	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		19	20	21	dB
SVRR	supply voltage ripple rejection	note 3				
	on		48	–	–	dB
	mute		48	–	–	dB
	standby		80	–	–	dB
$ Z_i $	input impedance		50	60	75	$k\Omega$
V_{no}	noise output voltage					
	on	$R_s = 0\ \Omega$; note 4	–	50	–	μV
	on	$R_s = 10\ \Omega$; note 4	–	70	100	μV
	mute	note 5	–	50	–	μV
α_{cs}	channel separation	$R_s = 10\ \Omega$	40	–	–	dB
$ \Delta G_v $	channel unbalance		–	0.1	1	dB

Notes

- Output power is measured directly at the output pins of the IC.
- Frequency response externally fixed.
- Ripple rejection measured at the output with a source impedance of $0\ \Omega$, maximum ripple amplitude of 2 V (p-p) and a frequency between 100 Hz and 10 kHz.
- Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
- Noise output voltage independent of R_s ($V_i = 0\text{ V}$).

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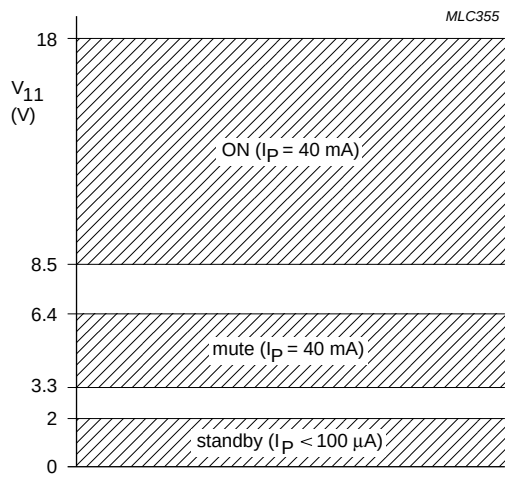


Fig.5 Standby, mute and on conditions.

APPLICATION INFORMATION

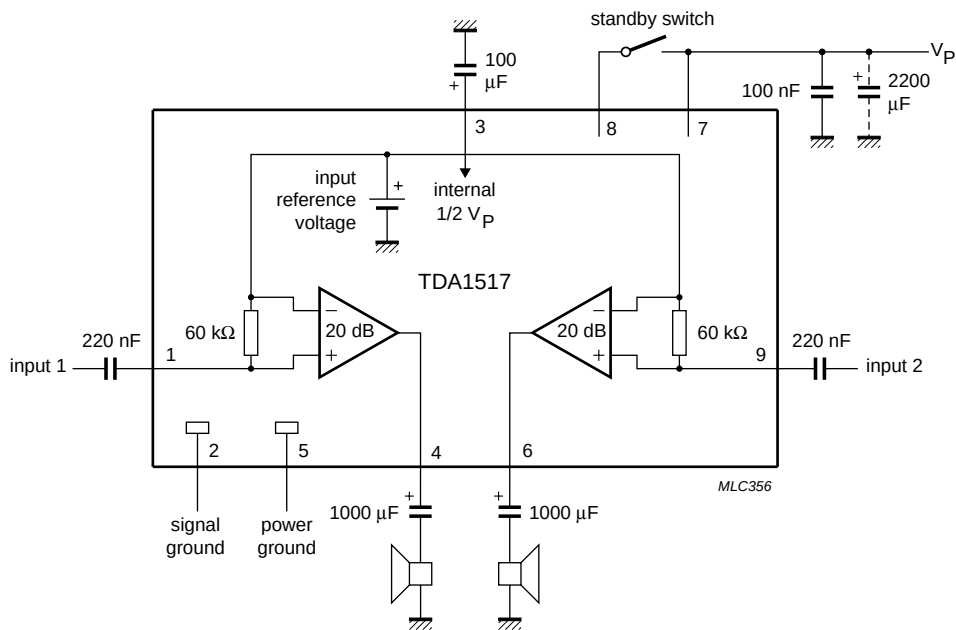


Fig.6 Application circuit diagram.

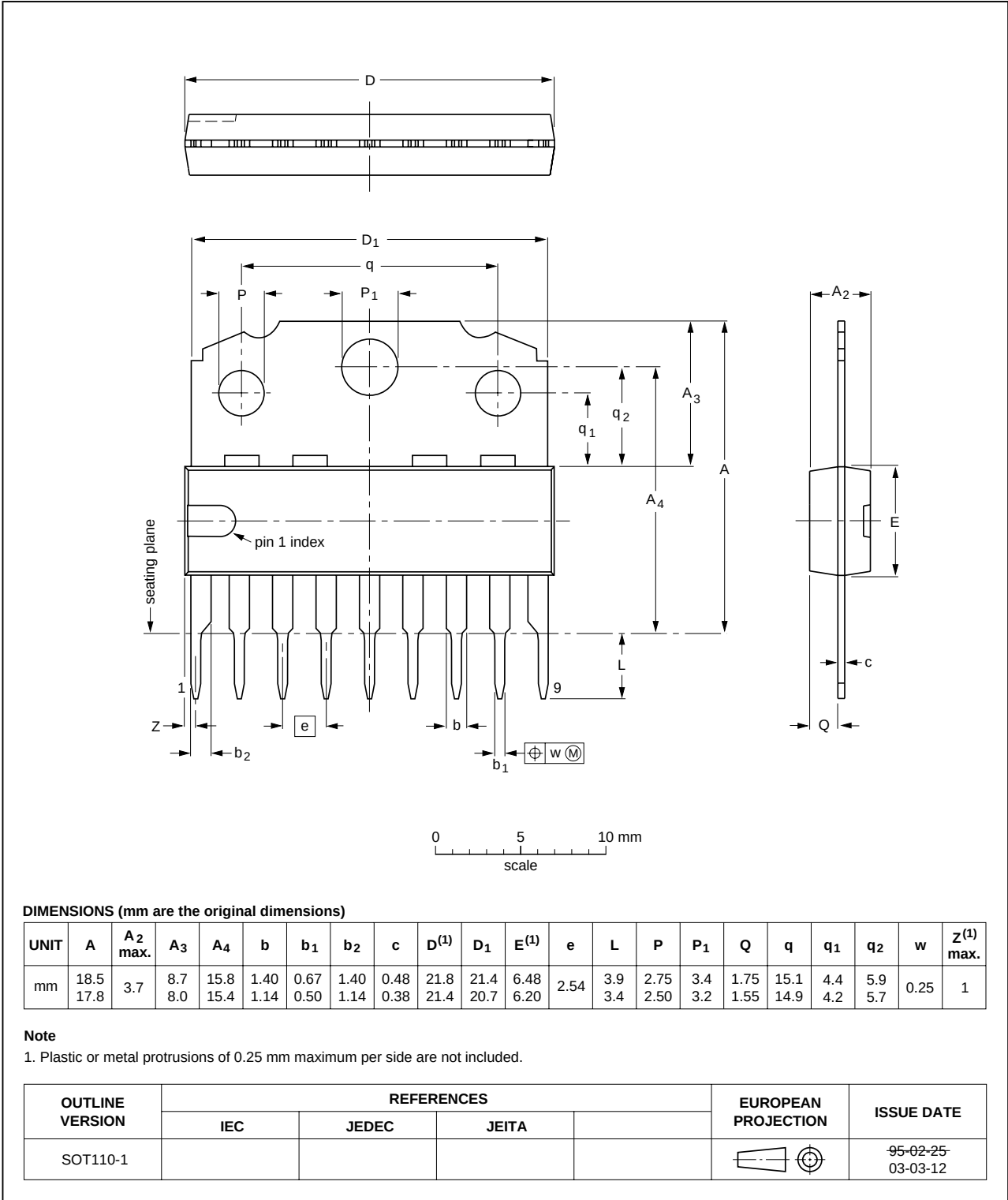
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PACKAGE OUTLINES

SIL9MPF: plastic single in-line medium power package with fin; 9 leads

SOT110-1

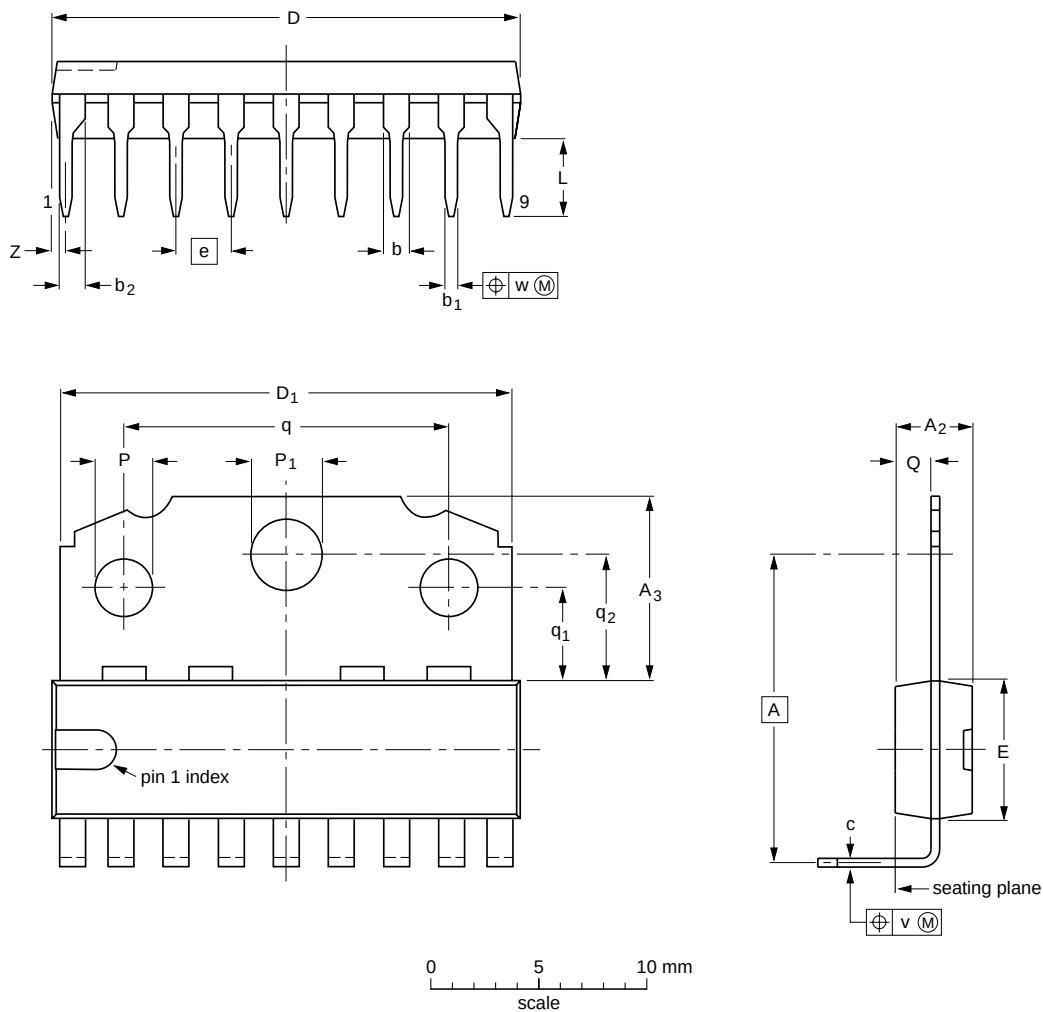


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RBS9MPF: plastic rectangular-bent single in-line medium power package with fin; 9 leads

SOT352-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₂ max.	A ₃	b	b ₁	b ₂	c	D ⁽²⁾	D ₁	E ⁽²⁾	e	L	P	P ₁	Q	q	q ₁	q ₂	v	w	z ⁽²⁾ max.
mm	14.45 13.95	3.7	8.7 8.0	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.8 3.3	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.6	0.25	1

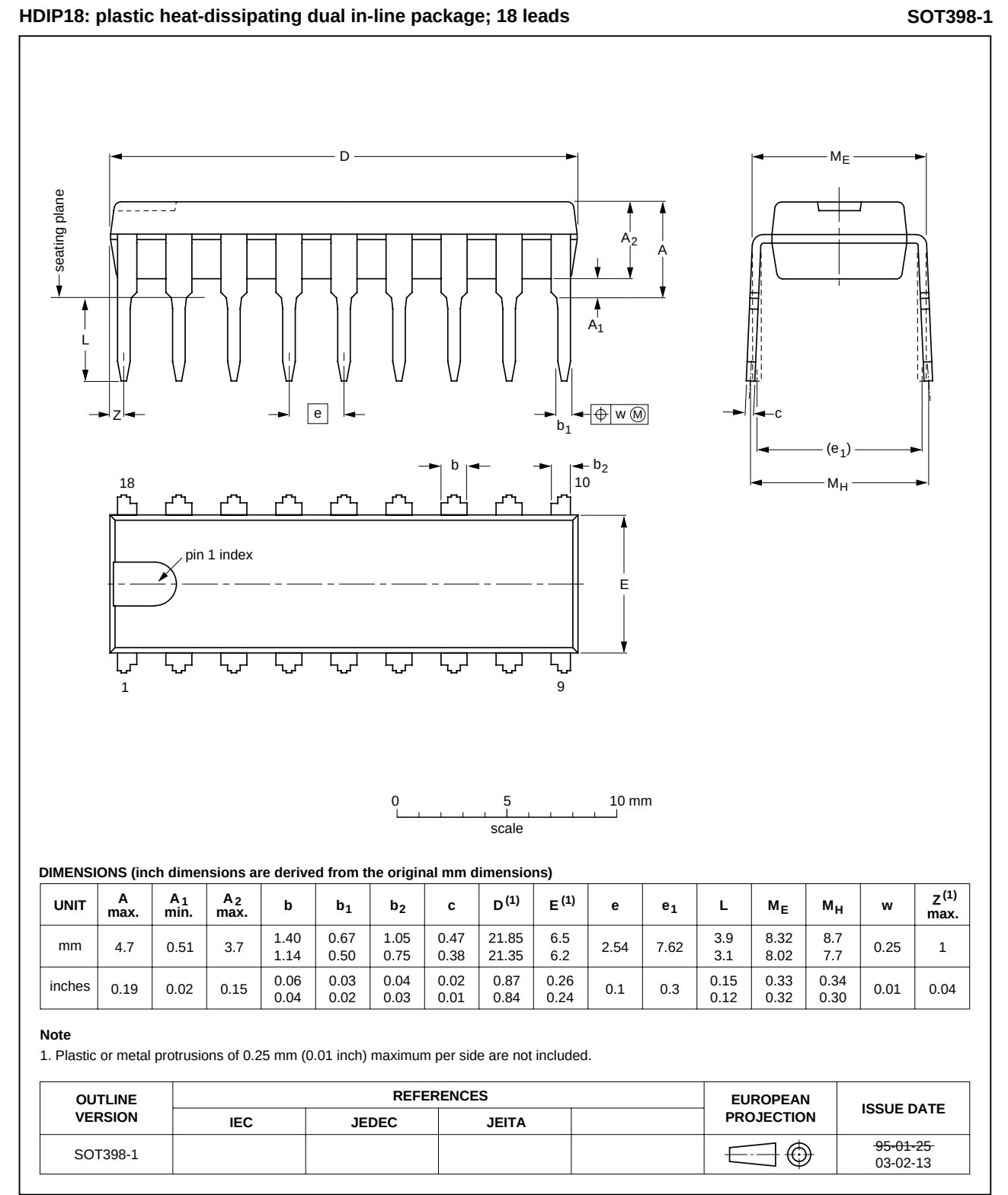
Notes

- 1. Dimension is specified at seating plane.
- 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT352-1						97-12-16 03-03-12

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SOLDERING**Introduction to soldering through-hole mount packages**

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{\text{stg(max)}}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
CPGA, HCPGA	–	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable ⁽¹⁾
PMFP ⁽²⁾	–	not suitable

Notes

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
- For PMFP packages hot bar soldering or manual soldering is suitable.

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
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